**L.D. College of Engineering**

**Information Technology Department**

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| **Teaching Scheme** |
| **Theory** | **Tutorial** | **Practical** | **Total** |
| **04** | **00** | **02** | **06** |

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| **Subject Name:** | **Digital Electronics** | **Duration: 18/06/2018 to 17/10/2018** |
| **Subject Code:** | **2131004** |  |
| **Branch & Semester:** | **III-IT – A** |  |

**Name of Faculty: Prof. A. C. Patel**

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| **Sr.No.** | **Topic Name** | **Proposed Date** | **Actual Date** |
|  | **Boolean Algebra and Mapping Methods:** |  |  |
| **1** | Boolean Algebra,  | **18/6 22/6** |  |
| **2** | Karnaugh Maps, Variable Entered Maps,  | **25/6 29/6**  |  |
| **3** | Realizing Logic Function with Gates,  | **2/7 6/7**  |  |
| **4** | Combinational Design Examples. | **9/7**  |  |
|  |  |  |  |
|  | **Flip Flops, Counters and Registers:**  |  |  |
| **1** | **Flip Flops** | **13/7 16/7 20/7 23/7** |  |
| **2** | **Applications** | **27/7 30/7 3/8 6/8** |  |
|  |  |  |  |
|  | **Synchronous State Machine Design:**  |  |  |
| **1** | Sequential Counters,  | **10/8 13/8**  |  |
| **2** | State Changes Referenced to Clock,  | **20/8**  |  |
| **3** | Number of State Flip-Flops,  | **24/8 27/8 31/8**  |  |
| **4** | Input Forming Logic, Output Forming Logic,  | **3/9 7/9**  |  |
| **5** | Generation of a State Diagram from a Timing Chart, Redundant States,  | **10/9 14/9** |  |
| **6** | General State Machine Architecture | **17/9 24/9** |  |
|  |  |  |  |
|  | **Logic Families:** |  |  |
| **1** | Transistor-Transistor Logic(TTL),  | **28/9** |  |
| **2** | Emitter-Coupled Logic(ECL),  | **1/10**  |  |
| **3** | MOSFET Logic,  | **5/10** |  |
| **4** | TTL Gates | **8/10** |  |