L. D. College of Engineering, Ahmedabad – 15

LESSON PLAN

Over all Term Planning	
Branch:	Information Technology
Semester:	B.E 3RD SEM
Subject Name:	Digital Electronics
Subject Code:	2131004
Affiliating University:	Gujarat Technological University
Starting date of the term:	18-06-2018
Ending date of the term:	17-10-2018
Course Teacher:	Prof. N. P. Desai

University Structure of the subject:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks			Practical Marks			
L	T	P	C	ESE (E)	PA (M)		ESE (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Sr No	Contents	Total Hours	% Weightage
1	Binary Systems and Logic Circuits: The Advantage of Binary, Number Systems, The Use of Binary in Digital Systems, Logic Gates, Logic Family Terminology.	3	5
2	Boolean Algebra and Mapping Methods: Boolean Algebra, Karnaugh Maps, Variable Entered Maps, Realizing Logic Function with Gates, Combinational Design Examples.	7	15
3	Logic Function Realization with MSI Circuits: Combinational Logic with Multiplexers and Decoders, Standard Logic Functions with MSI Circuits, Design Problem Using MSI Circuits.	7	15

4	Flip Flops, Counters and Registers: Flip Flops and its Applications	8	15
5	Introduction to State Machines: The Need for State Machines, The State Machine, Basic Concepts in State Machine Analysis.	3	5
6	Synchronous State Machine Design: Sequential Counters, State Changes Referenced to Clock, Number of State Flip-Flops, Input Forming Logic, Output Forming Logic, Generation of a State Diagram from a Timing Chart, Redundant States, General State Machine Architecture	8	15
7	Asynchronous State Machines: The Fundamental-Mode Model, Problems of Asynchronous Circuits Basic Design Principles, An Asynchronous Design Example.	7	15
8	Logic Families: Transistor-Transistor Logic(TTL), Emitter-Coupled Logic(ECL), MOSFET Logic, TTL Gates.	4	5
9	Programmable Logic Devices: Introduction to Programmable Logic Devices, Read-Only Memory, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Combinational PLD-Based State Machines, State Machines on a Chip.	5	10
Total		**52**	

Reference Books:

1. Digital Logic & State Machine Design By David J. Comer, Third Indian Edition, Oxford University Press
2. Digital Logic and Computer Design By M Morris Mano, Fourth Edition, Prentice Hall Publication
3. Digital Principles and Applications By Malvino & Leach, Seventh Edition, McGraw-Hill Education
4. Modern Digital Electronics By R.P.Jain, Fourth Edition, Tata McGraw-Hill Education.
5. Digital Electronics: Principles and Integrated Circuits By A.K. Maini, Wiley India Publications
6. Digital Design M. Morris Mano and Michael D. Ciletti, Pearson Education
7. Digital Electronics and Design with With VHDL, Volnei A. Pedroni, Elsevier (Morgan Kaufmann Publishers)

Lesson Plan

Sr. No.	Topic	Planned Date (Div A)	Actual Date (Div A)	Planned Date (Div B)	Actual Date (Div B)	Mode of Delivery	Resources required
1	The Advantage of Binary, Number Systems,			25/6/2018		Chalk Board/ppt	Hand Outs/ppt

2	The Use of Binary in Digital Systems, Logic Gates,			2/7/2018		Chalk Board/ppt	Hand Outs/ppt
3	Logic Family Terminology			10/7/2018		Chalk Board/ppt	Hand Outs/ppt
4	Combinational Logic with Multiplexers and Decoders,			17/7/2018		Chalk Board/ppt	Hand Outs/ppt
5	Standard Logic Functions with MSI Circuits,			30/7/2018		Chalk Board/ppt	Hand Outs/ppt
6	Design Problem Using MSI Circuits.			6/8/2018		Chalk Board/ppt	Hand Outs/ppt
7	The Need for State Machines, The State Machine,			14/8/2018		Chalk Board/ppt	Hand Outs/ppt
8	Basic Concepts in State Machine Analysis.			27/8/2018		Chalk Board/ppt	Hand Outs/ppt
9	The Fundamental-Mode Model, Problems of Asynchronous Circuits			4/9/2018		Chalk Board/ppt	Hand Outs/ppt
10	Basic Design Principles, An Asynchronous Design Example.			11/9/2018		Chalk Board/ppt	Hand Outs/ppt
11	Introduction to Programmable Logic Devices,			24/9/2018		Chalk Board/ppt	Hand Outs/ppt
12	Read-Only Memory, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL),			1/10/2018		Chalk Board/ppt	Hand Outs/ppt
13	Combinational PLD-Based State Machines, State Machines on a Chip.			15/10/2018		Chalk Board/ppt	Hand Outs/ppt

Lab Planning

Sr. No.	Exercise Title	Planned date of performance	Equipment's Required	Materials Required	Remarks
1	AIM: To study about various Basic Gates and other Gates.				
2	AIM: Configuring NAND and NOR logic gates as universal gates.				
3	AIM: To Prove De Morgan's Theorem using				

	Truth Tables.				
4	AIM: To implement Binary to Gray and Gray to Binary Code Converter.				
5	AIM: To Study and configure various digital circuits such as Half adder, Full adder, half subtractor and Full subtractor.				
6	AIM: To Study and configure Decoders & Encoders				
7	AIM: To Study and configure MUX and DEMUX.				
8	AIM: To study & verify SR and D – Flip Flops with Truth table				
9	AIM: To study & verify JK and T – Flip Flops with Truth table				
10	AIM: To study & implement Magnitude Comparator.				
11	AIM: To study Simulator and its components				
12	AIM: To study and configure Register & Counter.				

Prof. N. P. Desai

Department of Information Technology

L. D. C. E. – Ahmedabad-15